

Technical Specifications (In-Cash Procurement)

Technical specification of the framework contract for Advanced Protection System development

This document defines the technical requirements for the provision of technical and engineering services to support the design, development and system V&V of the ITER Central Interlock System's Fast Architecture (CIS-FA) and specifically the Advanced Protection System (APS). The support services will be ordered under a framework service contract by means of task orders and shall be performed at the Contractor premises.

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1 Purpose

This document defines the technical requirements for the provision of technical and engineering services to support the design, development and system V&V of the ITER Central Interlock System's Fast Architecture (CIS-FA) and specifically the Advanced Protection System (APS). The support services will be ordered under a framework service contract by means of task orders and shall be performed at the Contractor premises.

2 Scope

The scope of the services is to support the design, development and system V&V for APS based on CIS-FA.

3 Definitions

APS	Advanced Protection System
CIS	Central Interlock System
CIS-CG	CIS Critical Gateway
CIS-FA	CIS Fast Architecture
CIS-PPM	CIS Plasma Protection Module
CODAC	Control, Data Access and Communication
C-R	Contractors Contract Responsible
DMA	Direct Memory Access
DMS-PIS	Disruption Mitigation System Plant Interlock System
DRC	Design Rules Check (applicable to a specific FPGA device)
FAT	Factory Acceptance Test
FP	First Plasma
FPGA	Field Programmable Gate Array
F-PIS	Fast Plant Interlock System
IDM	ITER Document Management
IO	ITER Organization
IO-RO	ITER Organization Responsible Officer
IO-TRO	ITER Organization Technical Responsible Officer
N/A	Not Applicable
OTS	Off-the shelf
PAR	Place and Route
PFPO-1	Post First Plasma Operation (Phase 1)
QA	Quality Assurance
RD	Reference Documents
SAT	Site Acceptance Test
SAT	Site Acceptance Tests
SDN	ITER Synchronous Data Network
SFF	Safe Failure Fraction
STA	Static Timing Analysis
SVN	ITER CODAC SubVersion

V&V Verification & Validation

For a complete list of ITER abbreviations see: ITER Abbreviations (ITER_D_2MU6W5).

4 References

	Document	Reference	Version
[RD1]	General Management Specification for Service and Supply (GM3S)	ITER_D_82MXQK	1.4
[RD2]	PBS-46 DDD	ITER_D_PNYY53	4.3
[RD3]	SDG-45 - Software Development Guideline for CODAC	ITER_D_YDKRGN	1.0
[RD4]	Plant Control Design Handbook	ITER_D_27LH2V	7.0
[RD5]	TO4 documentation : PFCS F-PIC functions, Overrides, Simulation template and SPI data publishing	ITER_D_N6D3NM	1.0
[RD6]	Sub-System Requirement Document (s-SRD) 46.01.AP (Advanced Protection System)	ITER_D_A7DD4T	1.1
[RD7]	Requirements for CIS Critical Gateway	ITER_D_32J4EU	2.4
[RD8]	Memo on the functional architecture of CIS pulse termination	ITER_D_A74FWN	1.8
[RD9]	Assessing NI FPGA-based platform with MXIe interface for use in ITER hard real-time investment protection applications	IEEE_TNS'24	
[RD10]	MARTe2 Code and User Documentation	MARTe2	
[RD11]	MARTe2-components Code and User Documentation	MARTe2-components	
[RD12]	Overview of the TCV digital real-time plasma control system and its applications.	link	
[RD13]	Quality Classification Determination	ITER_D_24VQES	5.5
[RD14]	MARTe2 QA procedures	contributing.html	
[RD15]	cRIO investment protection manual	ITER_D_88BPRY	TBA
[RD16]	System Engineering Management Plan	ITER_D_2F68EX	3.5
[RD17]	PCS design plan	ITER_D_RCAAUF	3.1
[RD18]	APS Functional Architecture	ITER_D_54QU9X	1.2
[RD19]	CIS Critical Gateway (prototype) host application	ITER_D_9FH9ZD	1.0
[RD20]	CIS Critical Gateway (prototype) firmware	ITER_D_8Z3KXN	1.2
[RD21]	Data point structures & interfaces for CIS-CG	ITER_D_AVVSAR	latest

5 Technical Context

5.1 Framework Goals

The main goal of this framework is to deliver four Advanced Protection System (APS) sub-systems that are required operational from the start of ITER super-conducting magnet commissioning and auxiliary heating systems integrated commissioning.

The framework includes design and development of host-software, firmware and test-bench for each system. Supporting verification activities for components used in the realisation of each system and preliminary system validation (Factory Acceptance Test). The framework excludes verification activities for final system release, site acceptance testing and commissioning.

This framework is to be read in combination with the General Management Specification for Service and Supply (GM3S) – [RD1] that constitutes a full part of the technical requirements.

In case of conflict, the content of the framework supersedes the content of [RD1].

5.2 System Overview

The APS is part of the ITER Interlock Control System (ICS), which oversees the investment protection (or otherwise known as machine protection) mechanisms at ITER through automated execution of interlock functions. As well as the APS, ICS comprises of the Central Interlock System (CIS) and Plant Interlock Systems (PIS).

The APS [RD6] [RD18] is in charge of computing hybrid (physics-related) protection functions over the state-space of the tokamak. The different PIS are in charge of the protection functions local to each plant, and the CIS implements the coordination logic part of central interlock functions, in between the event generating PIS/APS and actuating PIS/APS [RD2]. The APS is primarily an event generating system, except in the case of ITER's disruption mitigation system (DMS) where it operates in a control role. To execute its functions, and unless stated otherwise for specific subsystems, the APS integrates tightly with ITER's diagnostic systems via CODAC.

The APS is intended to be implemented using the CIS-Fast Architecture (CIS-FA) design baseline. This design relies heavily on FPGAs to guarantee certain hard real-time requirements as explained in Section 5.4. CIS-FA systems combine a PC-Host and NI-cRIO FPGA connected via PCI Express. The FPGAs are tasked with executing the fail-safe part of the protection functions, while interfacing to CIS and PIS. The PC-Hosts are tasked with executing supporting functions like configuration, status monitoring, logging state-changes to the CIS central logging system.

For the specific case of APS, CIS-FA systems will be permitted to receive conventional inputs through real-time Ethernet connections of the PC-Host. Consequently, system designs need to compartmentalise risks from the use of these interfaces and to ensure there is adequate isolation between critical and non-critical functionalities.

5.3 Standards

The CIS-FA is evaluated as Quality-Class-1 (QC-1) in the ITER quality classification determination [RD13], this classification drives the overall Quality Assurance (QA) Requirements behind Section 13 and is a step-up from the conventional systems [RD3].

The main requirements for the CIS-FA stem from the ITER Plant Control Design Handbook [RD4] Section 6, which bases its recommendations on the IEC61508 standard. APS protection functions are classified by their safety integrity level which ranges from SIL-1 to SIL-3. System validation and verification requirements are to be commensurate with these ratings.

Notwithstanding of the reliability target, the main concern of CIS-FA is ITER investment protection and not safety. Therefore, in applying IEC61508, there is the standing requirement that the contractor & IO shall take adequate care to re-interpret & document IEC61508 goals with their new concern. In some cases, the goals might be irrelevant to investment protection, or they might be beyond adequate demonstration given the novelty of certain ITER investment protection functions. Moreover, it needs to be noted that the IEC61508 best-practice¹ w.r.t. FPGA design is not sufficiently concrete. IO also uses IEC62566 as an additional reference to obtain best-practice for high-criticality FPGA development. If the IO development guidelines are not clear, the contractor has the responsibility to point out where these need to be elaborated, dropped or made more concrete. The contractor is also responsible to document the decisions that were taken in that regard in coordination with IO. IO typically takes decisions on the merit that a certain goal brings definitive improvements to reliability, availability and maintainability of a system.

¹ Particularly Part-2 Annex-F

Specific to the quality of firmware, IO conducted extensive research into techniques & measures that can be applied over NI LabVIEW-FPGA generated firmware. These results are summarised in [RD15] and constitute the overall V&V plan IO would like to follow in that regard. The work description in Section 6, leans on the workflows identified in that document. The framework aims to execute all activities with the exception for the final firmware release stage and associated V&V.

Concerning host-side software development, the MARTe2 real-time framework is covered by its own QA procedure [RD14]. This QA procedure follows IEC61508-3 to a certain extent. However, (as detailed later) the contractor will be requested to carry out additional confidence building measures in areas where the QA procedure has unacceptable gaps w.r.t. IEC61508-3 for certain MARTe2 components.

Any situation which is not covered by the existing hardware architecture guidelines and firmware development guidelines the contractor shall refer to IEC61508/IEC62566 and coordinate a decision with IO as per the standing requirement described earlier.

5.4 Overview of CIS-FA

This section provides a description of the CIS-FA to facilitate a better understanding of the scope of works and services described in Section 6.

A CIS-FA node consists of two hosts and two NI9159 chassis as shown in Figure 1.

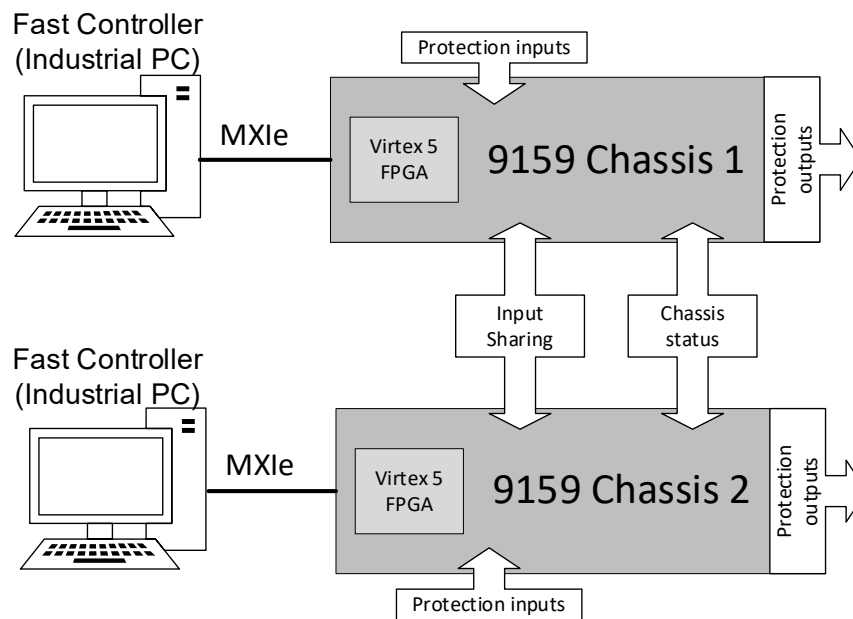


Figure 1 CIS-FA double-decker subsystem

Each National Instruments chassis contains a Xilinx Virtex-5 LX100 FPGA. A pair of host and chassis are geographically separated from another pair to ensure high availability during emergency situations like fires, earthquakes and other common-cause issues. The two chassis form a 1oo2D protection train, where “D” stands for “diagnostic”. As per this design, the chassis perform runtime checks, share inputs and internal status so they can jointly decide on the protection outputs. The design aims at reducing infrastructure requirements while maintaining similar availability to a 2oo3. The downside of a 1oo2D is that the firmware can be more complex. CIS-FA designs aim to achieve over 90% safe-failure fraction (SFF) and a hardware fault-tolerance of at least one.

The protection outputs from the system can be short data-packets using 5V TTL or 24 V digital control signals. The fail-safe state of each chassis is to stop/power-off its own protection outputs, leaving the other chassis in charge of protection for the short period until the tokamak is brought

to a state where the affected protection functions are no longer required. This is done by signaling conventional control systems to terminate the pulse in an emergency stop [RD8].

The design requires that protection logics and runtime diagnostics be implemented on the FPGAs for assurance reasons. The software running on the host is responsible for loading firmware, acquiring interlock status from the FPGA via a target-to-host (T2H) Direct Memory Access (DMA), interfacing data-logging/Human Machine Interface (HMI) support systems and integrating the node into ITER's Concept of Operation. The software also sends configuration parameters for the interlocks through a host-to-target (H2T) DMA. The FPGA treats this interface as a black-channel (see IEC61508-2), meaning that it can detect a large proportion of errors with the data stream, and can reject the configuration parameters should it detect that there is an error. Subsequently, configuration parameters are stored in distributed memory banks which are continuously compared before using them in a protection loop.

The FPGAs are time-synchronized to within a worst-case of 5usec and a 1usec jitter from ITER TCN. Although not a correctness criterion for the majority of hard real time protections, the time-synchronization is needed for accurately evaluating cause-and-effect through a chain of these controllers. The systems can support a minimum accuracy for reporting the state of interlocks to within 500usec of TCN. Below this limit, the status of interlocks can be buffered and sent via the T2H DMA which provides a bandwidth of 8MB/s.

In the case of the APS, the host must execute semi-trusted protection codes and interface conventional systems like diagnostics. The functional architecture of an APS node intends that these codes will process complex measurements for the determination of plasma state in real-time. However, to maintain the properties of the original design and to integrate with ICS, the core protection logic and the trusted runtime diagnostics are to be implemented on the FPGA. Towards this purpose, the CIS-FA design was upgraded to utilize the MARTe2 real-time framework [RD10] and components [RD11].

Additionally, the host-side application interfaces to SCADA and central data-logging systems through OPC UA.

On the backbone CIS-FA 1oo2D architecture, functions with higher redundancy ratings can be implemented with the NI C-Type I/O modules. These are documented as different design patterns for each type of module and pure logic function. The designs patterns require adaptation to specific systems like APS.

For more information refer to the CIS-FA hardware architecture guidelines [RD5], the firmware development guidelines [RD15] and the CIS Critical Gateway prototype development [RD19][RD20][RD21], which is closest in complexity to APS.

6 Scope of Works and Services

The work developing APS sub-systems is split in stages that follow a V-development lifecycle [RD16]. This overall management plan is adjusted for the particularities of system design with FPGA-based real-time systems like CIS-FA.

Specifications for ITER protection functions are formalised via the ITER Machine Protection Panel and drafted into function specifications. Functional specifications, detail a certain fault tolerance and reliability target. In the specific case of APS functions, the functional requirements are further verified in the control domain and will be handed over in the form of Simulink models [RD17].

These (core) requirements are then extended with:

- requirements for system interfaces,
- requirements for failure detection and fault-tolerance,

- requirements for the inclusion of standardized support functions converting system configuration [RD12] & data logging.

The result is a detailed system requirements document for an APS sub-system that IO provides to the contractor as part of a task specification to develop the system. An example is [RD7]. The main task for the contractor is to develop the system using the design patterns described and to produce a test-stand for the system.

6.1 List of tasks

6.1.1 *Deliver improvements to design methodology*

Tasks in this section will request that the contractor deliver certain improvements that will make system delivery more efficient. Similar to the way MARTe2 is deployed on the TCV tokamak [RD12], the contractor will be requested to review this method and to provide guidelines, tools and recommendations for a tighter integration of PCSSP Simulink (model) and CIS-FA (node).

The goal is to facilitate:

- Capturing the data points for a given system and generating the required MARTe2 structures for serving the data points over OPC UA.
- Capturing of the host & firmware interface and generating the required MARTe2 structures such that traceability between Simulink signals, host application and firmware can be kept consistent and maintained.
- Rules the PCSSP Simulink developer should follow to facilitate the mapping of functionalities to various constituent parts of the CIS-FA node.

Tasks in the scope of this section will also request certain additional confidence building measures to be performed over MARTe2 or its components, such as expert code reviews, dynamic or static analysis.

6.1.2 *Overall design of a given APS sub-system*

Tasks in this section, will aim to consolidate the activities from three distinct tracks of activities for each APS subsystem that shall be developed:

- a) The host side application design and development.
- b) The firmware design and development.
- c) Development of a test bench and end-to-end system testing.

The contractor is expected to establish a concrete host-application/firmware interface (like [RD21]) and to prioritise the development of firmware that implements this interface. The latter is needed to start host-side application development as there is no emulator for NI9159 that can support host-side application development. Outside of this coordination point, work on the three aspects above can take place independently from one another and might have to be executed in parallel to meet development schedules.

Description of services required:

1. Assessment of the functional specifications and participate in drafting a detailed design document for a system. Such documents need to cover at least:
 - a. The input/response times of each element in the generalised protection function.
 - b. The required control cycle time for the host and firmware parts.
 - c. The interface requirements of the protection function to the rest of CIS.
 - d. The main configuration parameters and the critical configuration parameters.
 - e. The definition for the interface between host and firmware.

2. Drafting of a system integration report which documents specific requirements that have been achieved with the list components for the host-application and firmware at specific versions.
3. Drafting the system validation procedure will contain a description of the test bench and will act as requirements for its development.

Deliverables:

- Input into detailed system requirements for APS subsystem,
- Integration report for APS subsystem.
- System validation procedure for an APS subsystem

6.1.3 Host-side application design & development

Tasks in this section, will aim to deliver the host-side software for a given APS subsystem.

As mentioned earlier the host-side application development for the APS is based on the real-time framework MARTe2 running on a Linux PREEMPT_RT kernel. Additionally, IO has developed and tested bespoke Linux drivers for the NI9159, that aim to deliver the kind of hard real-time requirements APS subsystems might have [RD9].

MARTe2 has a significant number of pre-developed components which are integrated into an application in a data-driven manner. Towards system design, the contractor shall be expected to:

- decide which MARTe2 components to use to realise system functions,
- determine the host-side data-interfaces,
- determine real-time constraints and plan the control-flow and data-flow accordingly,
- identify resultant failure modes and ensure these are detectable and lead to predictable fail-safe behaviour for the entire system,
- achieve a separation between critical and non-critical parts of the host-side application.

Towards system development, the contractor might have to re-engineer certain MARTe2 components or to develop specific components for a given APS sub-system. These tasks are carried out in C/C++'98. However, the majority of the expected work is on realising the designs through the MARTe2 configuration mechanism.

For complex APS physics algorithms, the contractor shall be permitted to resort to MATLAB/Simulink code generation, integrating the code via the MARTe2 SimulinkWrapperGAM. Additional verification activities for performing such an integration will be given as a specific task.

Description of services required:

1. Identification & development of the MARTe2 components necessary to realise the host-side application.
2. Vulnerability-analysis into supporting library components and recommendations for MARTe2 components based on them.
3. Rapid prototyping of parts of a system to establish consistency & feasibility of firmware requirements & design and documenting results with the overall logic-solver V&V reports.
4. Input into the preparation of the system V&V plan.
5. Input into the preparation of the system integration plan.

Deliverables:

- Implementation report of a new MARTe2 component,
- Unit-test procedure for a MARTe2 component,

- Architecture of the APS Structural Magnet Protection System host-side application,
- Architecture of the APS Magnet Overheat Protection System host-side application,
- Architecture of the APS Limits and Pulse Enable Windows host-side application,
- Architecture of the APS Electron Cyclotron Heating Limits system host-side application,
- Input into system validation procedure for each of the systems above.

6.1.4 Firmware design & development

Tasks in this section, will aim to deliver the firmware for a given APS subsystem.

Firmware design & development is characterised by integration of pre-developed building blocks into a LabVIEW-FPGA firmware for a given APS sub-system through a LabVIEW FPGA workflow.

Building blocks covering core system functions like time synchronization, Manchester code/decode, H2T/T2H DMAs (to interface MARTe2) and configuration parameter management will be provided by IO. These are intended to be integrated along patterns that give a certain concretion on the overall firmware architecture. The contractor is expected to develop and integrate building blocks for implementation of system-specific functions. The contractor may develop such blocks in LabVIEW-FPGA, VHDL or vetted IP cores.

Requirements for the development of building blocks vary by their type and the integrity level they are intended to support. The overall scope is as follows:

- The block must have a requirements document that is approved by IO or issued by IO.
- The block must have a user manual stating integration requirements and limitations on use.
- The user manual of a building block based on an IP core must be adapted for the particular intended use within ITER ICS generally or APS subsystem specifically.
- Building blocks based on subVI must meet a certain coding standard.
- Building blocks based on subVI must not depend on encrypted subVIs,
- IO must own the licences of any IP core that the contractor intends to use.
- Building blocks based on VHDL must respect a certain coding ruleset, and the specifics to LabVIEW FPGA integration must be respected.
- All building blocks must have an example integration project.
- Demonstration that the generated or user-defined VHDL conforms to the expected timing requirements,
- Checking for constraints on project delivery structure.

Description of services required:

1. Detailed firmware requirements and architecture,
2. Provide input in the preparation firmware V&V plan.
3. Development of building blocks in LabVIEW and in VHDL.
4. Configuring Xilinx IP-cores after reviewing their documentation.
5. Fast-prototyping of LabVIEW elements to close unknowns in a given development plan.
6. Integrate building blocks into a firmware for a given APS sub-system.

Deliverables:

- Architecture of the APS Structural Magnet Protection System firmware.
- Architecture of the APS Magnet Overheat Protection System firmware.

- Architecture of the APS Limits and Pulse Enable Windows firmware.
- Architecture of the APS Electron Cyclotron Heating Limits system firmware.
- Integration report for the firmware of a given system.
- Codes for a specific building block of a firmware.

6.1.5 *End-to-end system testing and development of a test bench*

Tasks in this section, will aim to deliver a test bench for the APS subsystem and may execute the system validation procedures.

APS subsystems development requires end-to-end system testing at two points in the life-cycle.

- a) Determining that a certain version of host-application and firmware is ready to undergo a release stage,
- b) Formal system validation (also known at ITER as factory acceptance test FAT or SAT).

Primarily, the contractor will be expected to develop system test benches for each APS sub-system. Generally, a system test bench consists of the system under test and a third host & NI9159 pair that can provide stimuli to the system under test and sample its outputs (as shown in Figure 2). Test benches may also be developed using newer cRIO platforms such as NI9049. The detailed requirements for a test-bench are expected to come from test procedures developed as part of Section 6.1.2. This might require that the test-bench host integrate MATLAB/Simulink models for stimuli generation.

The system test-bench is expected to use the same core technologies as the system under test. However, its development can rely on a larger set of components that do not need to be vetted to the same degree of confidence as the ones used in the system under test.

Description of services required:

- Configuration control,
- Drafting of adequate test procedures,
- Linux system administration,
- Version control through SVN and GIT.

Deliverables:

1. Test-bench description for a given APS sub-system.
2. Test-report for a given APS sub-system (i.e. the result from executing a test procedure)

The work in developing the test-bench is expected to take place at the contractor's premises. For sensitive investment protection systems IO may delegate the execution of the test procedure to a different contractor or send an expert witness to the contractor's premises. This may impact certain Task Orders in this framework, requiring that the test results show successful delivery of the required functionality.

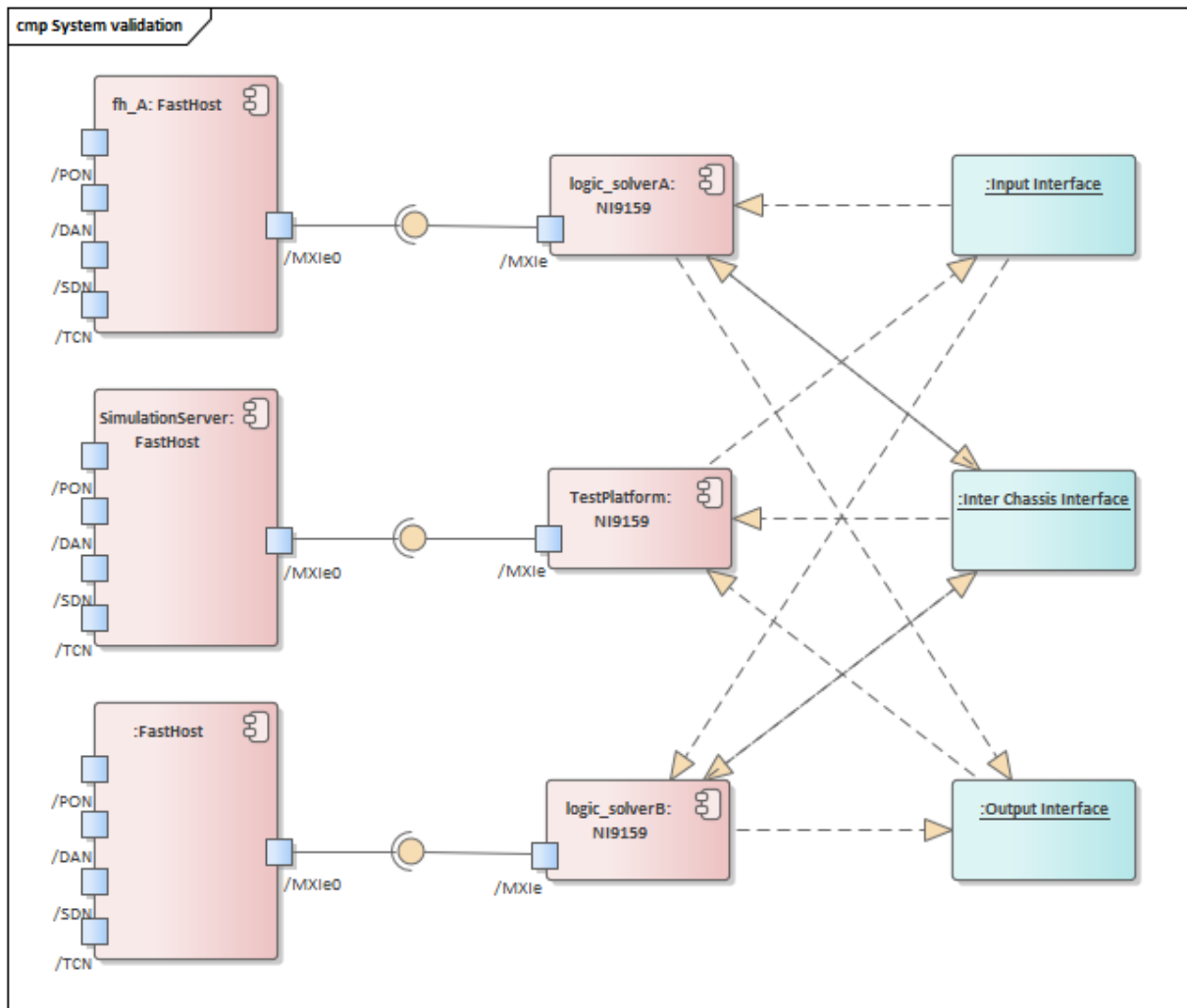


Figure 2 System oriented tests

7 Required competencies

- [REQ-1] Clear, precise, unambiguous documentation writing in English.
- [REQ-2] Test plans writing that are verifiable, testable, and feasible.
- [REQ-3] Knowledge of IEC61508, IEC61511 and IEC62566.
- [REQ-4] Experience with C/C++'98 development.
- [REQ-5] Experience with Doxygen.
- [REQ-6] Practical experience with real-time applications on a Linux operating system (pthreads & RT_PREEMPT kernel).
- [REQ-7] Practical experience with PCI Express Specification and Linux PCIe drivers.
- [REQ-8] Experience in MATLAB/Simulink and its code generation capabilities.
- [REQ-9] Experience with python and/or shell scripting.
- [REQ-10] Experience with Xilinx ISE, ISE IP cores and VHDL/HDL development.

- [REQ-11] Experience with Xilinx Virtex-5 architecture and documentation (or similar Xilinx FPGA).
- [REQ-12] Experience with LabVIEW - FPGA v2017.
- [REQ-13] Experience with expert code review in both C/C++ and VHDL/HDL.
- [REQ-14] Experience of static analysis of C/C++, MISRA-C++:2008 and static analysis of VHDL/HDL.
- [REQ-15] Configuration management and best practices using SVN and GIT.
- [REQ-16] Understanding of parser technology (optional).
- [REQ-17] Use of Enterprise Architect for system design (optional).
- [REQ-18] Practical experience with Linux administration (optional).
- [REQ-19] Understanding of WinCC OA/OPC UA based SCADA systems (optional).
- [REQ-20] Experience with TCL scripting (optional).
- [REQ-21] Experience with simulation test-benches in SystemVerilog (optional).
- [REQ-22] Experience with Xilinx constraint files (optional).
- [REQ-23] Experience with unit-testing in C++ and continuous integration environments Jenkins (optional).

8 Estimated duration

The duration of services under this Contract will be four (4) years fixed plus one (1) year optional.

9 Responsibilities

9.1 Contractor's Responsibilities

The work will be performed according to deliverables defined in Task Orders. In order to successfully perform the tasks in these Task Orders, the Contractor shall:

- Nominate a Contract Manager to be responsible for the execution of the Contract and its follow-up including contacts, meetings and progress reports throughout the duration of the Contract.
- Strictly implement the IO procedures, instructions and document templates.
- Provide experienced and trained resources to perform the tasks.
- Contractor's personnel shall possess the qualifications, professional competence and experience to carry out services in accordance with IO rules and procedures.
- Contractor's personnel shall be bound by the rules and regulations governing the IO ethics, safety and security IO rules.

9.2 IO's Responsibilities

The IO shall:

- Nominate a Responsible Officer (IO-RO) to manage the Contract;
- Provide office desks at IO premises during on-site work, if such is required.

- Make available procedures, information, data, any specialized equipment and tools necessary for the Contractor to perform its functions under the scope of work.

Any IT IO account creation is to be requested by IO-RO. The account duration should be limited to the required usage of the account (e.g. contract duration).

10 Acceptance Criteria

The following criteria shall be the basis of the acceptance of the successful accomplishment of the work.

Reports and design documentation as deliverables shall be stored in the IO's document management system, IDM by the Contractor for acceptance. A named IO's Contract Technical Responsible Officer is the Approver of the delivered documents. The Approver can name one or more Reviewers(s) in the area of the report's expertise. The Reviewer(s) can ask modifications to the report in which case the Contractor must submit a new version. The approval of the document by the delivery due date as set in the Task Order is a required acceptance criterion.

Additional acceptance criteria shall be stipulated within Task Orders, related to software, firmware and verification reports.

11 Specific Requirements and Conditions

The work will be performed at the Contractor's premises.

The Contractor is responsible to provide the necessary tools for administrative work for all staffs working at their premises.

The Contractor shall have and maintain the necessary equipment and licenses to run the software tools required to carry out the engineering analyses and produce the deliverables in accordance with the tools adopted by the IO. IO will grant access for the Contractor's staff to IDM when appropriate.

IO can grant temporary local licences for LabVIEW 2017-FPGA to the contractor but the hardware to run LabVIEW will need to be provided by the contractor.

IO can provide MATLAB 2024b licences, but the contractor will need to use IO infrastructure through NoMachine.

To facilitate good communication, the Contractor shall have access to screen sharing tools, e.g. Microsoft Teams, and the necessary equipment compatible with IO facilities.

All results obtained in the frame of the work described in this document shall be made property of the ITER Organization and can be partially or fully used for further work.

12 Contract Execution & Organisation

12.1 Work Monitoring / Meeting Schedule

As a general statement, the details of the services to be provided by the Contractor will be defined in the task order technical specification documents.

12.1.1 Contract Meetings

For the purposes of this contract, the following meetings are defined:

12.1.1.1 Kick-Off Meeting

The IO shall organize a Kick-Off Meeting (KoM) within two weeks after the contract signature. The KoM may take place in IO premises or remotely by video-conference if required by the IO. The following topics will be presented:

- General context of the contract;
- Main activities and deliverables to be produced by the Contractor.

12.1.1.2 Monthly Meetings

The Contractor shall organise monthly meetings in IO premises or remotely by video-conference if required by the IO for:

- General contract progress.
- Summary of the work carried out and the resources used.
- Identification of any issues in the contractual process, and
- Planning of Contractor's resources for the following months.

The Contractor Contract Manager shall participate in the monthly meetings. The minutes of these meetings shall be written by the Contractor in the simplified form of a table of action items and archived in ITER Document Management system (IDM).

12.1.1.3 Ad-hoc Meetings

To be scheduled at the discretion of the IO-RO or the Contractor depending on need. The minutes of these meetings shall be written by the Contractor in the simplified form of a table of action items and archived in IDM.

12.1.2 Progress Reports

The Contractor shall submit written progress reports to the IO Responsible Officer every month. The progress report shall be in .doc(x) format and include at least the following information for the reporting period:

- Summary of the work carried out for all on-going Task Orders.
- Description of any problems encountered for all on-going Task Orders.
- References to any produced deliverables for all on-going Task Orders.
- Status and schedule of all on-going Task Orders.

Progress reports shall be submitted three working days before regular meetings and discussed there. The submission of these reports shall be performed using IDM. The progress report shall be approved by the IO-RO.

12.2 Payment Schedule

The Contractor shall supply invoices to IO at completion of a Task Order or at specified payment milestones within a Task Order. The Contractor shall send the invoices only after the corresponding deliverables have been approved by the IO-RO.

13 Quality Assurance (QA) Requirements

The organisation conducting these activities should have an ITER approved QA Program or an ISO 9001 accredited quality system.

The general requirements are detailed in [ITER_D 22MFG4 - Quality Requirements for IO Performers](#). Prior to commencement of the task, a Quality Plan must be submitted for IO approval giving evidence of the above and describing the organisation for this task; the skill of workers

involved in the study; any anticipated sub-contractors; and giving details of who will be the independent checker of the activities (as in [ITER_D_22MFG4 - Quality Requirements for IO Performers](#)).

Documentation developed as the result of this task shall be retained by the performer of the task or the DA organization for a minimum of 5 years and then may be discarded at the direction of the IO. The use of computer software to perform a safety basis task activity such as analysis and/or modelling, etc. shall be reviewed and approved by the IO prior to its use, in accordance with [Quality Assurance for ITER Safety Codes \(ITER_D_258LKL\)](#).

14 Safety Requirements

ITER is a Nuclear Facility identified in France by the number-INB-174 (“Installation Nucléaire de Base”).

In application of the Article 14 of the ITER Agreement, for nuclear safety, the French Nuclear Regulation must be observed. The contractor must implement necessary provisions for the application of the Order 7th February 2012.

In such case the Suppliers and Subcontractors must be informed that:

- The compliance with the INB-order must be demonstrated in the chain of external contractors.
- The contractor must comply with all the requirements expressed in [RD1] Section 5.3.
- For each requirement, the contractor must explain in its quality system the dispositions taken to implement requirements stipulated in [RD1] Section 5.3.

Activities of this framework may be considered PIA. Each task order will specify which activities are to be considered PIA.